

SRM UNIVERSITY
FACULTY OF ENGINEERING AND TECHNOLOGY

SCHOOL OF COMPUTING
DEPARTMENT OF CSE
COURSE PLAN

Course Code : CS0207
Course Title : Computer Organization and architecture
Semester : III
Course Time : Jul – Nov 2009

Day	F	
	Hour	Timing
Monday	-	-
Tuesday	2	9.20-10.10
Wednesday	2,6	9.20-10.10,2.20-3.10
Thursday	5	1.30-2.20
Friday	-	-

Location : S.R.M.E.C – Tech Park

Faculty Details

Sec.	Name	Office	Office hour	Mail id
F	SENTHIL KUMAR .G	Tech Park	Monday - Friday	gsenthilkumar@cse.srmuniv.ac.in

Required Text Books:

1. Carl Hamacher, "Computer Organization", Fifth Edition, McGrawHill International Edition, 2002
2. P.Pal Chaudhuri, "Computer Organization and Design", 2nd Edition, PHI ' 2003
3. William Stallings, "Computer Organization and Architecture – Designing for Performance", PHI, 2004.
4. John P.Hayes, "Computer Architecture and Organization", III Edition, McGraw Hill International Editions, 1998.

Web resources

www.amazon.com

www.freebookcentre.com

Prerequisite : CS0102 – Digital computer fundamentals

Objectives

1. Gives a knowledge of various architectures
2. CPU, Control unit, I/O Processing
3. Memory and its types
4. Design of the above components

Assessment Details

Cycle Test – I	:	10 Marks
Surprise Test – I	:	7 Marks
Cycle Test – II	:	10 Marks
Surprise Test – II	:	8 Marks
Model Exam	:	15 Marks

Test Schedule

S.No.	DATE	TEST	TOPICS	DURATION
1		Cycle Test - I	Unit I & II	2 periods
2		Cycle Test - II	Unit III & IV	2 periods
3		Model Exam	All 5 units	3 Hrs

Outcomes

Students who have successfully completed this course will have full understanding of the following concepts

Course outcome	Program outcome
To learn The basic functional units, operational concepts and The basic memory operations, addressing modes. Basic ALU functions (operations) Control unit design and memory and its types Input and output processing – bus interface I/O interface	An ability to understand the basic functioning of computer. To understand the concepts of addressing modes a To solve various ALU operations. To implement booth algorithm To understand various types of memory concepts I/O processing.

Detailed Session Plan

UNIT-I INTRODUCTION					
Evolution of Computer Systems-Computer Types-Functional units-Basic operational concepts-Bus structures-Memory location and addresses-memory operations- Addressing modes-Design of a computer system-Instruction and instruction sequencing, RISC versus CISC					
Sessi on No.	Topics to be covered	Time (min)	Ref	Teaching Method	Testing Method
1	Evolution of Computer Systems	50	1,2	BB	Group discussion Quiz
2	Computer Types	50	1,2	BB	Objective type test Quiz
3	Functional units	50	1	BB	Quiz
4	Basic operational concepts, Bus structures	50	1	BB	Quiz
5	Memory location and addresses-memory operations	50	1,3	BB	Quiz
6	Addressing modes	50	1,3	BB	Quiz Objective type test

7	Design of a computer system	50	2	BB	Quiz, Assignment
8	Instruction and instruction sequencing	50	1,3	BB	Group discussion
9	RISC versus CISC	50	1,3	BB	Group discussion
UNIT-II CENTRAL PROCESSING UNIT					
Introduction-Arithmetic Logic Unit - Fixed point arithmetic, floating point arithmetic-Execution of a complete instruction-Basic concepts of pipelining					
10	Introduction-Arithmetic Logic Unit	50	1,2	BB	Quiz
11	Fixed point arithmetic	50	1,2	BB	Quiz Brain storming
12	Fixed point arithmetic	50	1,2	BB	Quiz Surprise Test
13	Floating point arithmetic	50	1,2	BB	Group discussion Quiz
14	Floating point arithmetic	50	1,2	BB	Group discussion, Quiz
15	Floating point arithmetic	50	1,2	BB	Quiz, Assignment
16	Execution of a complete instruction	50	1,2	BB	Quiz
17	Basic concepts of pipelining	50	1,2	BB	Quiz
18	Basic concepts of pipelining	50	1,2	BB	Quiz
UNIT-III CONTROL UNIT DESIGN					
Introduction-Control Transfer-Fetch cycle - Instruction Interpretation & Execution - Hardwired control - Microprogrammed control					
19	Introduction-Control Transfer	50	2	BB,PPT	Quiz Group discussion Objective type test
20	Fetch cycle	50	2	BB,PPT	Quiz Group discussion
21	Fetch cycle	50	2	BB,PPT	Quiz
22	Instruction Interpretation & Execution	50	1,2	BB,PPT	Quiz Surprise Test
23	Instruction Interpretation & Execution	50	1,2	BB,PPT	Quiz Group discussion
24	Hardwired control	50	1,2	BB,PPT	Quiz
25	Hardwired control	50	1,2	BB,PPT	Quiz Group discussion
26	Microprogrammed control	50	1,2	BB,PPT	Quiz
27	Microprogrammed control	50	1,2,3	BB,PPT	Quiz Brain storming
UNIT-IV MEMORIES AND SUBSYSTEMS					
Semiconductor memory - Static and Dynamic -Associative memory- Cache memory- Virtual memory- Secondary memories-Optical magnetic tape & magnetic disks & controllers					
28	Semiconductor memory- Static and Dynamic memory	50	1,2,3	BB	Group discussion Assignment
29	Static and Dynamic memory	50	1,2,3	BB	Group discussion Quiz
30	Associative memory	50	1,2,3	BB	Group discussion

					Assignment
31	Associative memory	50	1,2,3	BB	Group discussion Assignment
32	Cache memory	50	1,2,3	BB	Objective type test Quiz Group discussion
33	Virtual memory	50	1,2,3	BB	Quiz Group discussion
34	Secondary memories-Optical magnetic tape	50	1,2,3	BB	Objective type test
35	Magnetic disks & controllers	50	1,2,3	BB	Objective type test
36	Magnetic disks & controllers	50	1,2,3	BB	Quiz Group discussion
UNIT-V I/O PROCESSING					
Introduction-Data transfer techniques- Bus Interface- I/O Channel-I/O Processor, I/O devices -Direct memory access.					
37	Introduction-Data transfer techniques	50	1,2	BB	Group discussion
38	Bus Interface	50	1,2	BB	Objective type test
39	I/O Channel	50	1,2	BB	Brain storming
40	I/O Processor	50	1,2	BB	Brain storming
41	I/O Processor	50	2,3	BB	Surprise test Quiz
42	I/O devices	50	2,3	BB	Assignment
43	I/O devices	50	2,3	BB	Assignment
44	Direct memory access.	50	1,2	BB	Brain storming
45	Direct memory access.	50	1,2	BB	Brain storming