SRM UNIVERSITY
FACULTY OF ENGINEERING AND TECHNOLOGY

SCHOOL OF COMPUTING
DEPARTMENT OF CSE
COURSE PLAN

Course Code : CS0205
Course Title : MICROPROCESSOR & INTERFACING
Semester : IV
Course Time : JULY – DEC 2009

Day	SECTION									
	A		B		C		D		E	
	Hour	Timing	Hour	Timing	Hour	Timing	Hour	Timing	Hour	Timing
Monday	-	-	1	8.30 - 9.20	-	-	2	9.20 – 10.10	-	-
Tuesday	7	3.10 – 4.00	-	-	1,5	8.30-9.20, 1.30 – 2.20	-	-	2	9.20-10.10
Wednesday	1	8.30 -9.20	2	9.20 – 10.10	7	3.10 – 4.00	4	11.10 – 12.00	2,6	9.20-10.10,2.20-3.10
Thursday	-	-	-	-	4	11.10 – 12.00	3	10.20 – 11.10	5	1.30-2.20
Friday	1 5	8.30 -9.20 1.00 – 1.50	1, 5	8.30 - 9.20 & 1.30 – 2.20	-	-	4	11.10 – 12.00	-	-

Location : S.R.M.E.C – Tech Park

Faculty Details:

Sec.	Name	Office	Office hour	Mail id
A	Mr.S.Selvakumar	Tech Park	Tuesday, Wednesday & Friday	Selva_harur@yahoo.co.in
B	Mrs. E. Poovammal	Tech Park	Monday, Wednesday & Friday	poovammal@cse.srmuniv.ac.in
C	Mr. A.Murugan	Tech Park	Tuesday, Wednesday & Thursday	amurugan@cse.srmuniv.ac.in
D	Mr.T Peermeeralabbai	Tech Park	Monday, Wednesday, Thursday,Friday	Peermeera@cse.srmuniv.ac.in
E	Akilandeswari.P	Tech Park	Monday - Friday	akilandeswari@cse.srmuniv.ac.in

Required Text Books

1. Ray A K, K M Bhurchandi, "*Advanced Microprocessor & Peripherals",* Tata McGraw Hill,1st Edition,2000
2. Ramesh S. Gaonkar, "*Microprocessor Architecture, Programming and Applications with the 8085*",Penram International Pub, 3rd Edition, 1997
3. Douglas V Hall, "*Microprocessor & Interfacing*", Tata McGraw Hill, 2nd Edition,1999.
4. Rafiquzzuman M, "*Microprocessor theory & Applications*", Prentice Hall of India,1994.
5. Yuchenhiu, Glenn A Gibson, "*Microprocessor Systems - 8086/8088 Family*", Prentice Hall of India, 2nd Edition, 1986.

Web resources

1. www.emu8086.com
2. www.cpu-world.com
3. www.hobbyprojects.com
4. www.8052.com

Pre-requisite : NIL

Objectives :

In this course, students learn the following topics:

1. Architecture of 8086 & 8088 microprocessors
2. Instruction sets of 8086/88 and programming.
3. Math Coprocessor & I/O processor and multiprocessor configuration
4. Interfacing of microprocessor with various peripheral devices

Assessment Details :

Cycle Test – I	:	10 Marks
Surprise Test – I	:	7 Marks
Cycle Test – II	:	10 Marks
Surprise Test – II	:	8 Marks
Model Exam	:	15 Marks

Test Schedule :

S.No.	DATE	TEST	TOPICS	DURATION
1	**As per Calendar**	**Cycle Test - I**	**Unit I & II**	**2 periods**
2	**As per Calendar**	**Cycle Test - II**	**Unit III & IV**	**2 periods**
3	**As per Calendar**	**Model Exam**	**All 5 units**	**3 Hrs**

Outcomes :

Students who have successfully completed this course will have full understanding of the following concepts

Course outcome	Program outcome
To learn about Microprocessor 8085 Architecture & Instructions	An ability to understand the basic functioning of 8085 and do programs
Microprocessor 8086 Architecture & Instructions	An ability to understand the basic functioning of 8086 and do programs
Communication Interfaces	An ability to design memory systems, and do programs for communication and peripheral interfacing
Peripheral Interfaces	
Multiprocessor systems	An ability to understand the basic functioning of multiprocessor systems

Detailed Session Plan :

INTEL 8085 ARCHITECTURE

Introduction to 8085 - 8085 architecture- Instruction Set & Assembler Directives- Assembly Language Programming with 8085.

Session No.	Topics to be covered	Time (min)	Ref	Teaching Method	Testing Method
1	Introduction to 8085	50	2	BB/PP	Discussion Quiz
2	8085 architecture	50	2	BB/PP	Quiz
3	Addressing modes, Instruction Set	50	2	BB/PP	Quiz
4	Instruction Set	50	2	BB/PP	Quiz
5	Assembler Directives	50	2	BB/PP	Quiz
6	Assembly Language Programming with 8085.	50	2	BB/PP	Discussion Objective type test
7	Assembly Language Programming with 8085.	50	2	BB/PP	Discussion Objective type test
8	Assembly Language Programming with 8085.	50	2	BB/PP	Discussion Objective type test
INTEL 8086/8088 ARCHITECTURE Introduction to 8086/8088 - 8086/8088 architecture- Instruction Set & Assembler Directives- Assembly Language Programming with 8086/8088- Special Architectural Features.					
9	Introduction to 8086/8088	50	1,5	BB/PP	Discussion
10	8086/8088 architecture	50	1,5	BB/PP	Discussion, Quiz
11	Instruction Set	50	1,5	BB/PP	Discussion Comparative Study
12	Instruction Set	50	1,5	BB/PP	Comparative Study
13	Assembler Directives	50	1,5	BB/PP	Quiz
14	Assembly Language Programming with 8086/8088	50	1,5	BB/PP	Quiz
15	Assembly Language Programming with 8086/8088	50	1,5	BB/PP	Quiz, Assignment

16	Special Architectural Features	50	1,5	BB/PP	Quiz Group discussion
COMMUNICATION INTERFACES Basic Peripherals & their interfacing with 8086/8088-Semiconductor Memory Interfacing-Dynamic RAM Interfacing-Interfacing I/O Ports-PIO 8255-Modes of Operation-Interfacing Analog to Digital Data Converters- Stepper Motor Interfacing					
17	Basic Peripherals & their interfacing with 8086/8088	50	1,5	BB	Discussion
18	Semiconductor Memory Interfacing	50	1,5	BB	Discussion
19	Semiconductor Memory Interfacing	50	1,5	BB	Tutorial
20	Dynamic RAM Interfacing	50	1,5	BB	Discussion
21	Interfacing I/O Ports	50	1,5	BB	Discussion
22	PIO 8255-Modes of Operation	50	1,5	BB/PP	Quiz
23	Interfacing Analog to Digital Data Converters	50	1,5	BB	Quiz
24	Stepper Motor Interfacing	50	1,5	BB	Discussion
25	Overview of communication Interfaces	50	1,5	BB/PP	Quiz
PERIPHERAL INTERFACES Special Purpose Programmable Peripheral Devices & their Interfacing-Programmable Interval Timer 8253- Programmable Interrupt Controller 8259A-DMA Controller 8257-DMA Transfers & Operations-Programmable DMA Interface 8237.					
26	Special Purpose Programmable Peripheral Devices & their Interfacing	50	3,4	BB	Discussion
27	Programmable Interval Timer 8253	50	3,4	BB/PP	Discussion
28	Programmable Interval Timer 8253	50	3,4	BB/PP	Quiz
29	Programmable Interrupt Controller 8259A	50	3,4	BB/PP	Discussion
30	Programmable Interrupt Controller 8259A	50	3,4	BB/PP	Quiz
31	DMA Controller 8257	50	3,4	BB/PP	Discussion
32	DMA Transfers & Operations	50	3,4	BB/PP	Discussion
33	DMA Transfers & Operations	50	3,4	BB/PP	Quiz
34	Programmable DMA Interface 8237	50	3,4	BB/PP	Discussion
35	Overview of Peripheral Interfaces	50	3,4	BB/PP	Objective type test Comparative study
MULTIPROCESSOR SYSTEMS Interconnection Topologies- Software Aspects of Multiprocessor Systems- Numeric Processor 8087- Bus Arbitration & Control- Tightly Coupled & Loosely Coupled Systems.					
36	Interconnection Topologies	50	1	BB/PP	Discussion
37	Software Aspects of Multiprocessor Systems	50	1	BB/PP	Discussion

38	Software Aspects of Multiprocessor Systems	50	1	BB/PP	Comparative study Assignment
39	Numeric Processor 8087- Data types & formats	50	1	BB	Discussion
40	8087 - Numeric Instruction Set	50	1	BB	Discussion, Quiz
41	Numeric Processor 8087 Stacks	50	1	BB	Quiz
42	Interface of Coprocessor (8087)	50	1	BB	Discussion
43	Bus Arbitration & Control	50	1	BB	Discussion
44	Tightly Coupled & Loosely Coupled Systems	50	1	BB/PP	Discussion
45	Overview of Multiprocessor System	50	1	BB/PP	Objective Type test

- BB – Black Board
- PP – Power Point