

SRM UNIVERSITY
FACULTY OF ENGINEERING AND TECHNOLOGY
SCHOOL OF ELECTRONICS AND COMMUNICATION ENGINEERING
DEPARTMENT OF ECE

Course Code : EC0223
Course Title : Digital Systems Lab
Semester : III
Course Time : Jul - Dec2009

Day	Section											
	A		B		C		D		E		F	
	Hr	Timing	Hr	Timing	Hr	Timing	Hr	Timing	Hr	Timing	Hr	Timing
Mon	2,3,4	9.00a.m. - 12.00 am			2,3,4	9.00a.m. - 12.00 am					5,6,7	1.30p.m. - 4.0p.m
Tue			2,3,4	9.00a.m. - 12.00 am			2,3,4	9.00a.m. - 12.00 am	5,6,7	1.30p.m-4.0p.m		
Wed			5,6,7	1.30p.m.-4.0p.m	5,6,7	1.30p.m.-4.0p.m						
Thu	5,6,7	1.30p.m.-4.0p.m					5,6,7	1.30p.m.-4.0p.m	2,3,4	9.00a.m. - 12.00 am	2,3,4	9.00a.m. - 12.00 am
Fri												

Venue : Digital Lab (Section A, B, E)
Integrated Circuits Lab (Section C, D, F)

Faculty Details

Sec.	Name	Office	Office hour	Mail id
A	Ms. E. CHITRA	Tech park: 803A	Monday (12.30 to 1.30)pm	chittu_76@yahoo.co.in
B	Ms. A. MARIA JOSSY	Tech park: 703A	Friday (12.30 to 1.30) pm	ajossy_iman@yahoo.co.in
C	Mr.M.S.BALAMURUGAN	Tech park: 706A	Friday (12.30 to 1.30) pm	balarayar@gmail.com
D	Ms. R. DAYANA	Tech park: 703A	Monday (12.30 to 1.30)pm	dayanaraj@rediffmail.com
E	Ms. V. SARADA	Tech park: 703A	Friday (12.30 to 1.30) pm	saradasaran@gmail.com
F	Mr.J.SELVAKUMAR	MB29	Friday (12.30 to 1.30) pm	selva2802@gmail.com

Required Text Books:

1. Morris Mano. M, “*Digital Design*“, Pearson education, Third Edition 2002.
2. Ronald J. Tocci, “*Digital System Principles and Applications*”, PHI, Sixth Edition, 1997.
3. Floyd, “*Digital Fundamentals*”, Universal Book Stall, New Delhi, 1986.
4. Morris Mano. M, “*Digital Design*“, PHI, Third Edition.
5. Ronald J. Tocci, “*Digital System Principles and Applications*”, Pearson education 9th edition.

Web Resources :

www.wikipedia.org, www.cs.ualberta.ca, www.eelab.usyd.edu, www.books.google, www.researchandmarkets.com
www.pdf-search-engine.com, www.freevideolectures.com

Prerequisite : EC0205 Digital Systems

Course objectives

This lab course is to provide an introduction to the characteristics of digital logic and the design, construction, testing and debugging of simple digital circuits.

Topics covered

- ? Introduction to design of simple logic circuits using logic gates
- ? Designing of an n bit ripple carry adder using full adder
- ? Designing of priority Encoder and Decoder
- ? Demultiplexer and implementing the Boolean function using MUX.
- ? flip-flops behavior using logic gates
- ? n-bit synchronous binary counters design
- ? n-bit asynchronous counters design
- ? shift registers design

Assessment Details

Labs will be graded as per the following grading policy:

Pre-Lab Work	20%
In-Lab Performance	30%
Post Lab Work	20%
Laboratory Report	30%

Outcomes

Students who have successfully completed this course

Course outcome	Program outcome
<ul style="list-style-type: none"> • Boolean Algebra An understanding of the basic operations and law of Boolean algebra An ability to construct a truth table for a Boolean expression An understanding of the minterms and maxterms of a Boolean algebraic expression • Combinational Logic An ability to implement a Boolean algebraic expression with digital logic gates An understanding of digital logic • Sequential Logic An ability to construct a timing diagram for a digital system An ability to implement basic synchronous sequential circuits with flip-flops An ability to derive the state table diagram from a sequential circuits • Digital Devices An understanding of the operation of logic gates An understanding of the operation of SR, T, JK, and D flip-flops An understanding of the operation of counters and registers an understanding of the operation of multiplexers, decoders. 	<p>The student will be able to apply the knowledge of mathematics, science, and engineering to solve the problems based on combinational digital logic systems</p> <p>The student will be able to identify and he will be able to solve the engineering programs based on sequential digital logic systems</p> <p>The student will have a broad knowledge in understanding the impact of engineering solutions in implementing Registers, Multiplexers and Counters.</p> <p>Ability to identify appropriate design specifications and to design solutions at the system, component, and/or process level using Digital ICs.</p>

Detailed Session Plan

Session No.	Name of the Experiment	References
1	Introduction to Combinational Design	Digital Design by M. Morris Mano (Ch:4), Digital Systems by Ronald J. Tocci(Ch:4)
2	Design of Binary Adder	Digital Design by M. Morris Mano (Ch:4), Digital Systems by Ronald J. Tocci(Ch:6)

3	Design of Magnitude Comparators	Digital Design by M. Morris Mano (Ch:4)
4	Design of Encoders and Decoders	Digital Design by M. Morris Mano (Ch:4), Digital Systems by Ronald J. Tocci(Ch:9)
5	Design of Multiplexer and Demultiplexer	Digital Design by M. Morris Mano (Ch:4), Digital Systems by Ronald J. Tocci(Ch:9)
6	Introduction to Sequential Design	Digital Design by M. Morris Mano (Ch:5), Digital Systems by Ronald J. Tocci(Ch:5)
7	Design of synchronous Counter	Digital Design by M. Morris Mano (Ch:6), Digital Systems by Ronald J. Tocci(Ch:7)
8	Design of Asynchronous Counter	Digital Design by M. Morris Mano (Ch:6), Digital Systems by Ronald J. Tocci(Ch:7)
9	Design of Shift Register	Digital Design by M. Morris Mano (Ch:6), Digital Systems by Ronald J. Tocci(Ch:5)

Draw Karnaugh maps and derive the necessary input equations for the JK FFs.

Give an example of a level sensitive storage device (a latch), and an edge sensitive storage device (a flip-flop). Explain the operation of each (draw timing diagrams).

what do Preset, Set and Clear do to a flip-flop? These are called Asynchronous inputs. How are they different from a Synchronous input?

How are the NOR implementation and the NAND implementations of an SR latch functionally different?

Sites reference vhdl

http://www.pldworld.net/hdl/2/-seas.upenn.edu/ese201/vhdl/vhdl_primer.html#Toc526061344
digital

<http://elm.eeng.dcu.ie/~digital1/ExamPapers/>

http://opencourseware.kfupm.edu.sa/colleges/ces/ee/ee200/files%5C7-Lab_manuals_EE200_Lab.pdf