CMOS FABRICATION

n – WELL PROCESS
Step 1: Si Substrate

Start with p-type substrate
Step 2: Oxidation

Exposing to high-purity oxygen and hydrogen at approx. 1000°C in oxidation furnace

SiO₂

p substrate
Step 3: Photoresist Coating

Photoresist is a light-sensitive organic polymer
Softens when exposed to light

[Diagram of a substrate with layers labeled Photoresist and SiO₂]
Step 4: Masking

Expose photoresist through n-well mask
Step 5: Removal of Photoresist

Photoresist are removed by treating the wafer with acidic or basic solution.
Step 6: Acid Etching

SiO$_2$ is selectively removed from areas of wafer that are not covered by photoresist by using hydrofluoric acid.
Step 7: Removal of Photoresist

Strip off the remaining photoresist

\[ \text{p substrate} \quad \text{SiO}_2 \]
Step 8: Formation of n-well

n-well is formed with diffusion or ion implantation
Step 9: Removal of SiO2

Strip off the remaining oxide using HF

wafer with n-well
Step 10: Polysilicon deposition

Deposit very thin layer of gate oxide using Chemical Vapor Deposition (CVD) process
Step 11: N- diffusion

N-diffusion forms nMOS source, drain, and n-well contact
Step 11: N- diffusion

Dopants were diffused or ion implanted

Strip off oxide
Step 12: P- diffusion

Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact.
Step 13: Contact cuts

The devices are to be wired together

Cover chip with thick field oxide

Etch oxide where contact cuts are needed
Step 14: Metallization

Sputter on aluminum over whole wafer

Pattern to remove excess metal, leaving wires
p-well CMOS process

The fabrication of p-well cmos process is similar to n-well process except that p-wells acts as substrate for the n-devices within the parent n-substrate
Advantages of n-well process

n-well CMOS are superior to p-well because of:

- lower substrate bias effects on transistor threshold voltage
- lower parasitic capacitances associated with source and drain region
- Latch-up problems can be considerably reduced by using a low resistivity epitaxial p-type substrate
- However, n-well process degrades the performance of poorly performing p-type transistor
Twin-Tub Process
LOGIC GATES
CMOS INVERTER
NAND Gate
NOR Gate
## Stick Diagram Colour Code

<table>
<thead>
<tr>
<th>Component</th>
<th>Colour Code</th>
</tr>
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<tbody>
<tr>
<td>P diffusion</td>
<td>Yellow/Brown</td>
</tr>
<tr>
<td>N diffusion</td>
<td>Green</td>
</tr>
<tr>
<td>Polysilicon</td>
<td>Red</td>
</tr>
<tr>
<td>Contacts</td>
<td>Black</td>
</tr>
<tr>
<td>Metal1</td>
<td>Blue</td>
</tr>
<tr>
<td>Metal2</td>
<td>Magenta/Purple</td>
</tr>
<tr>
<td>Metal3</td>
<td>Cyan/L.Blue</td>
</tr>
<tr>
<td>Component</td>
<td>Colour</td>
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<tr>
<td>---------------</td>
<td>--------</td>
</tr>
<tr>
<td>metal 1</td>
<td><img src="blue.png" alt="Blue" /></td>
</tr>
<tr>
<td>metal 2</td>
<td><img src="pink.png" alt="Pink" /></td>
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<tr>
<td>polysilicon</td>
<td><img src="red.png" alt="Red" /></td>
</tr>
<tr>
<td>n-diffusion</td>
<td><img src="green.png" alt="Green" /></td>
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<tr>
<td>p-diffusion</td>
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<tr>
<td>via</td>
<td><img src="gray.png" alt="Gray" /></td>
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</table>
NMOS transistor
PMOS transistor

layout

circuit symbol
INVERTER- STICK DIAGRAM
Two horizontal wires are used for connection with VSS and VDD. This is done in metal2, but metal1 can be used instead.
Step 2

Two vertical wires (pdiff and ndiff) are used to represent the p-transistor (yellow) and n-transistor (green).
Step 3

The gates of the transistors are joined with a polysilicon wire, and connected to the input.
Step 4

The drains of two transistor are then connected with metal1 and joined to the output. There cannot be direct connection from n-transistor to p-transistors.
Step 5

The sources of the transistors are next connected to VSS and VDD with metal1. Notice that vias are used, not contacts.
metal1 is used instead of metal2 to connect VSS and VDD supply
NAND Gate

NAND gate in CMOS
NOR Gate

NOR gate in CMOS
Layout Design Rules
<table>
<thead>
<tr>
<th></th>
<th>Description</th>
<th>Value</th>
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<tbody>
<tr>
<td>R1</td>
<td>Minimum active area width</td>
<td>3 L</td>
</tr>
<tr>
<td>R2</td>
<td>Minimum active area spacing</td>
<td>3 L</td>
</tr>
<tr>
<td>R3</td>
<td>Minimum poly width</td>
<td>2 L</td>
</tr>
<tr>
<td>R4</td>
<td>Minimum poly spacing</td>
<td>2 L</td>
</tr>
<tr>
<td>R5</td>
<td>Minimum gate extension of poly over active</td>
<td>2 L</td>
</tr>
<tr>
<td>R6</td>
<td>Minimum poly-active edge spacing</td>
<td>1 L</td>
</tr>
<tr>
<td></td>
<td>(poly outside active area)</td>
<td></td>
</tr>
<tr>
<td>R7</td>
<td>Minimum poly-active edge spacing</td>
<td>3 L</td>
</tr>
<tr>
<td></td>
<td>(poly inside active area)</td>
<td></td>
</tr>
<tr>
<td>R8</td>
<td>Minimum metal width</td>
<td>3 L</td>
</tr>
<tr>
<td>R9</td>
<td>Minimum metal spacing</td>
<td>3 L</td>
</tr>
</tbody>
</table>
R10  Poly contact size  2 L
R11  Minimum poly contact spacing  2 L
R12  Minimum poly contact to poly edge spacing  1 L
R13  Minimum poly contact to metal edge spacing  1 L
R14  Minimum poly contact to active edge spacing  3 L
R15  Active contact size  2 L
R16  Minimum active contact spacing  2 L
(on the same active region)
R17  Minimum active contact to active edge spacing  1 L
R18  Minimum active contact to metal edge spacing  1 L
R19  Minimum active contact to poly edge spacing  3 L
R20  Minimum active contact spacing  6 L
(on different active regions)
OTHER CMOS LOGIC