M.Tech (Full Time) – EMBEDDED SYSTEM TECHNOLOGY

Curriculum & Syllabus

(2015 – 2016)

Faculty of Engineering & Technology
SRM University
SRM Nagar, Kattankulathur – 603 203
M.TECH - EMBEDDED SYSTEM TECHNOLOGY (FULL TIME)
Curriculum & Syllabus
Batch 2015 – 2016 and onwards

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<tr>
<th>S. No.</th>
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Total Credits: 74

*Main Project-Phase I  **Main Project-Phase II

### Core courses

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<td>EM2001</td>
<td>Digital System Design and Testing</td>
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<td>EM2009</td>
<td>FPGA Design</td>
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### Program Electives

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### Supportive Courses

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### Other courses

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Learning design of digital circuits is a fundamental necessity for designing embedded systems. This subject provides necessary instruments to achieve that goal.

INSTRUCTIONAL OBJECTIVES

1. To impart knowledge on the theory of logic and logic functions.
2. To design digital circuits.
3. To learn fault diagnosis and testability algorithms.

UNIT I - ADVANCED TOPICS IN BOOLEAN ALGEBRA (13 hours)
Shannon’s Expansion theorem, Consensus theorem, Reed-Muller Expansion, Multiplexer logic as function generators, Design of static hazard-free and dynamic hazard-free logic circuits, Threshold logic, Symmetric functions.

UNIT II - SEQUENTIAL CIRCUIT DESIGN (12 hours)
Counters and Registers, Mealy and Moore machines, clocked synchronous sequential circuit design procedure-state diagrams-state table-state reduction-state assignment, Incompletely Specified Sequential Machines.

UNIT III - DESIGN WITH PROGRAMMABLE LOGIC DEVICES (11 hours)
Basic concepts, PROM as PLD, Programmable Array Logic (PAL), Programmable Logic Array (PLA), Design of combinational and sequential circuits using PLS’s, Complex PLD (CPLD), Introduction to Field Programmable Gate Arrays (FPGA), Xilinx FPGAs - Xilinx 3000 series and 4000 series FPGA.

UNIT IV - FINITE STATE MACHINES (FSM) (12 hours)
State Machine (SM) charts, Derivation of SM charts, Realization of SM charts, Linked State Machines, Architectures centered around Non-registered PLDs, State machine designs centered around shift registers, One-hot design method, Application of one-hot method.

UNIT V - FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS (12 hours)

REFERENCES
EM2002

MICROPROCESSORS AND MICRO CONTROLLERS

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Total Contact Hours – 75
Prerequisite: Nil

PURPOSE
To enable the student to understand the RISC (ARM) and CISC (Pentium) processors, which will be useful for designing high end embedded systems.

INSTRUCTIONAL OBJECTIVES
1. To learn RISC and CISC architectures of processors.
2. To learn ARM processor and its programming with Embedded C.
3. To learn to use ARM development tools and carry out experiments

UNIT I - MICROPROCESSOR ARCHITECTURE (9 hours)

UNIT II - HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM (9 hours)
The software model - functional description - CPU pin descriptions - RISC concepts - bus operations - Super scalar architecture - pipelining - Branch prediction - The instruction and caches - Floating point unit - protected mode operation - Segmentation - paging - Protection - multitasking - Exception and interrupts - Input/Output - Virtual 8086 model - Interrupt processing - Instruction types - Addressing modes - Processor flags - Instruction set - Basic programming the Pentium Processor. Lab exercise.

UNIT III - HIGH PERFORMANCE RISC ARCHITECTURE (24 hours)
ARM: The ARM architecture - ARM organization and implementation - The ARM instruction set - The thumb instruction set - Basic ARM Assembly language program - ARM CPU cores.

ARM DEVELOPMENT ENVIRONMENT
The AMULET asynchronous ARM Processors. Embedded Operating Systems - Principle Components – Application case study – VLSI Ruby II Advanced communication processor – nuvoTon Cortex M0 (Nu-LB-NUC140) Microcontroller processor & its supporting tools. Lab exercise

UNIT IV - INTRODUCTION TO EMBEDDED C AND APPLICATIONS (16 hours)
UNIT V: EMBEDDED OPERATING SYSTEMS(sEOS):
(17 hours)

REFERENCES
EM2003
EMBEDDED SYSTEM SOFTWARE

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Total Contact Hours – 60
Prerequisite: Nil

PURPOSE
Introduce the student with software concepts used in embedded systems.

INSTRUCTIONAL OBJECTIVES
1. To learn C language and assembly programming.
2. To learn Object orientation for programming and C++.
3. To learn software modeling fundamentals.

UNIT I - INTRODUCTION TO ASSEMBLY LANGUAGE AND DATA REPRESENTATION IN C (12 hours)

UNIT II - PROGRAMMING IN C (12 hours)

UNIT III - OBJECT ORIENTED PROGRAMMING (10 hours)
Object oriented analysis and design - C++ classes and objects – functions – data structures - examples.

UNIT IV - UNIFIED MODELING LANGUAGE (14 hours)

UNIT V - EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS (12 hours)
The compilation process – libraries – porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS - system design using RTOS.

REFERENCES
PURPOSE
Signal Processing is an upcoming embedded field wherein many small systems and robots are built with signal processing functions. This course gives an idea of signal processing concepts for embedded systems.

INSTRUCTIONAL OBJECTIVES
1. To learn DSP basics.
2. To know about typical DSP applications and their theory.
3. To learn DSP programming methods for small systems and related issues.

UNIT I - OVERVIEW OF DSP (14 hours)

UNIT II - DSP APPLICATIONS-I (10 hours)

UNIT III - DSP APPLICATIONS – II (9 hours)
Error correcting codes and channel coding, Hamming distance and error correction, CRC, Reed Solomon codes, convolution codes, Viterbi decoding, interleaving – practical issues in using DSP.

UNIT IV - DSP PROGRAMMING (15 hours)
Overview of DSP algorithms – DSP architectures – optimizing DSP software – RTOS for DSP, testing and debugging DSP systems – embedded DSP software design using multicore SoC architectures.

UNIT V - DSP PROGRAM OPTIMIZATION AND GUIDELINES: (9 hours)

REFERENCES
REAL TIME OPERATING SYSTEMS

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Total Contact Hours – 60
Prerequisite: Nil

PURPOSE
Real time operating systems are being widely used in many embedded systems. This course deals with the basics and typical RTOSs.

INSTRUCTIONAL OBJECTIVES
1. To learn fundamentals of operating system.
2. To study implementation aspects of real time concepts.
3. To study example RTOSs and applications.

UNIT I - RTOS PROGRAMMING FUNDAMENTALS: (12 hours)

UNIT II - RTOS FUNDAMENTALS: (10 hours)
Task management – Dual role of time – Intertask communication - Process input/output.

UNIT III - REAL TIME SCHEDULING: (11 hours)

UNIT IV - REAL TIME OPERATING SYSTEMS: (18 hours)
VX works - uCOS – POSIX standards - RT Linux – device drivers - Real time library of Keil IDE - RTOS Porting to a Target.

UNIT V - RTOS APPLICATION DOMAINS: (9 hours)
Case studies : Free-RTOS architecture - Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.

REFERENCES
4. VX works Programmers manual.
7. “Getting started with RT-Linux”, FSM Labs., Inc.,
EM2006

EMBEDDED SYSTEM ARCHITECTURE

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PURPOSE
To familiarize the student with the architecture of embedded systems in general.

INSTRUCTIONAL OBJECTIVES
1. To learn the rationale and concepts for designing embedded systems.
2. To know about typical engineering issues of software development.

UNIT I - INTRODUCTION TO EMBEDDED SYSTEMS (13 hours)
Embedded system model – embedded standards – block diagrams – powering the hardware - embedded board using von Neuman model.
EMBEDDED processors: ISA architecture models – application specific ISA models – general purpose ISA models – instruction level parallelism.

UNIT II - PROCESSOR HARDWARE (12 hours)

UNIT III - SUPPORT HARDWARE (12 hours)

UNIT IV - SOFTWARE (11 hours)

UNIT V - ENGINEERING ISSUES OF SOFTWARE (12 hours)
Design and development: architectural patterns and reference models – creating the architectural structures – documenting the architecture – analyzing and evaluating the architecture – debugging testing, and maintaining.

REFERENCES
**UNIT I - BASICS** (12 hours)

**UNIT II – SUPERSCALAR PROCESSORS** (13 hours)

**UNIT III - INSTRUCTION HANDLING** (13 hours)
Branch prediction, instruction fetching, register renaming, instruction scheduling, memory access instructions, back-end optimizations.

**UNIT IV - CACHE HIERARCHY** (10 hours)
L1 cache access – hiding memory latencies – large higher level caches – main memory.

**UNIT V - MULTIPROCESSING** (12 hours)

**REFERENCES**
PURPOSE
As the hardware is becoming more customizable it is essential for the embedded designer to know the fundamentals of VLSI design, to implement special function circuits used in embedded systems. Hence this course is offered.

INSTRUCTIONAL OBJECTIVES

1. To learn analysis of MOS transistor with all its relevant aspects to the static and dynamic operation.
2. To know principles of low power CMOS circuit design.
3. To learn basic hierarchical modeling concepts used in digital design.
4. To learn the four levels of abstraction – behavioral dataflow gate-level and switch-level.

UNIT I - MOS TRANSISTOR THEORY (15 hours)
MOS transistor theory introduction - Ideal V-I characteristics - second order effects- CMOS logic - CMOS fabrication and layout - VLSI design flow.

UNIT II - CIRCUIT CHARACTERIZATION & PERFORMANCE ESTIMATION (15 hours)
CMOS inverter - DC transfer characteristics- Delay estimation - logical effort - Power dissipation - scaling - latch up.

UNIT III - COMBINATIONAL AND SEQUENTIAL CIRCUIT DESIGN (15 hours)
Static CMOS - ratioed circuits - differential cascode voltage switch logic- Dynamic circuit - domino logic-pass transistor circuits - CMOS D latch and edge triggered flipflop - Schmitt trigger. Lab exercises.

UNIT IV - HDL PROGRAMMING USING BEHAVIORAL AND DATA FLOW MODELS (15 hours)
Verilog introduction - Typical design flow-Modules and ports-instances – components –lexical conventions - number specification - strings – identifiers and keywords –data types - System tasks and compiler directives - behavioral modeling - dataflow modeling - RTL - Gate level modeling - programs for combinational and sequential. Lab exercises

UNIT V - HDL PROGRAMMING WITH STRUCTURAL AND SWITCH LEVEL MODELS (15 hours)
Tasks and functions –difference between tasks and functions-switch level- MOS switches - CMOS switches- examples - CMOS NAND and NOR –MUX using transmission gate – CMOS flipflop.

REFERENCES
PRACTICAL WORKSHEET 1

LAB

L T P C  
FPGA SYSTEM DESIGN  3 0 2 4  
Total Contact Hours – 75
Prerequisite : Nil

PURPOSE
Complex and faster embedded systems can be made with FPGAs. This course introduces the design concepts of using FPGAs.

INSTRUCTIONAL OBJECTIVES
1. To learn FPGA architectures.
2. To learn and use design flow for using FPGA.
3. To learn programming of FPGA with practical circuits.

UNIT I - INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN (9 hours)
Types of ASICs - Design Flow - CMOS transistors, CMOS design rules - Combinational Logic Cell - Sequential logic cell - Data path logic cell - transistors as resistors - transistor parasitic capacitance - Logical effort - Library cell design - Library architecture.

UNIT II - PROGRAMMBLE LOGIC CELLS AND I/O CELLS (9 hours)
Digital clock Managers-Clock management - Regional clocks- Block RAM – Distributed RAM- Configurable Logic Blocks-LUT based structures – Phase locked loops- Select I/O resources –Anti fuse - static RAM - EPROM and EEPROM technology.

UNIT III - DEVICE ARCHITECTURES (15 hours)
Device Architecture-Spartan 6 -Vertex 4 architecture- Altera Cyclone and Quartus architectures.

UNIT IV - DESIGN ENTRY AND TESTING (21 hours)

UNIT V - FLOOR PLANNING, PLACEMENT AND ROUTING (21 hours)
System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow - global routing - detailed routing - special routing - circuit extraction – DRC.

REFERENCES
3. Design manuals of Altera, Xilinx and Actel.
PURPOSE
To introduce students with general concepts of computer architecture basics to enable them to use the processors effectively.

INSTRUCTIONAL OBJECTIVES
1. To familiarize with fundamentals of computer design.
2. To learn parallel and pipeline architectures.
3. To learn principles of parallel programming.

UNIT I - PROCESSOR AND MEMORY HIERARCHY (9 hours)
Multiprocessors and Multicomputers – Multivector and SIMD computers – Architectural Development Tracks – Processors and Memory Hierarchy – Advanced Processor Technology – Superscalar and vector Processor – Memory Hierarchy technology-Virtual memory technology.

UNIT II - FUNDAMENTALS OF COMPUTER DESIGN (9 hours)

UNIT III - PARALLEL AND SCALABLE ARCHITECTURES (9 hours)

UNIT IV - PIPELINING AND SUPER SCALAR TECHNIQUES (9 hours)

UNIT V - SOFTWARE FOR PARALLEL PROGRAMMING (9 hours)

REFERENCES
EM2102

EMBEDDED LINUX

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Total Contact Hours – 45
Prerequisite : Nil

PURPOSE
To enable the student to learn developing Linux based embedded applications.

INSTRUCTIONAL OBJECTIVES
1. To learn fundamentals of embedded linux.
2. To learn to use GNU tool chain.
3. To learn to implement embedded linux applications.

UNIT I - LINUX FUNDAMENTALS (9 hours)
Introduction - host-target development setup - hardware support - development languages and tools – RT linux.

UNIT II - INITIALIZATION (9 hours)
Linux kernel and kernel initialization - system initialization – hardware support - bootloaders.

UNIT III - DEVICE HANDLING (9 hours)
Device driver basics - module utilities - file systems - MTD subsystems – busybox.

UNIT IV - DEVELOPMENT TOOLS (9 hours)

UNIT V - DEVICE APPLICATIONS (9 hours)
Asynchronous serial communication interface - parallel port interfacing - USB interfacing - memory I/O interfacing - using interrupts for timing.

REFERENCES
PURPOSE
To introduce the design concepts of distributed embedded systems and CAN network, which is widely used in automotive and industrial embedded systems.

INSTRUCTIONAL OBJECTIVES
1. To understand the design principles of distributed embedded systems.
2. To learn CAN and CANopen networking.
3. To learn to design CAN network based systems.

UNIT I - REAL-TIME ENVIRONMENT (9 hours)
Real-time computer system requirements – classification of real time systems – simplicity – global time – internal and external clock synchronization – real time model.

UNIT II - REAL-TIME OPERATING SYSTEMS (6 hours)
Inter component communication – task management – dual role of time – inter task interactions – process input/output – agreement protocols – error detection.

UNIT III - SYSTEM DESIGN (12 hours)

UNIT IV - INTRODUCTION TO CAN (9 hours)
Introduction to CAN Open – CAN open standard – Object directory – Electronic Data Sheets & Devices.

UNIT V - CAN STANDARDS (9 hours)
Configuration Files – Service Data Objectives – Network management CAN open messages – Device Profile Encoder.

REFERENCES
PURPOSE
There is a need for designing hardware and software for data communication devices. This course aims at equipping the student with necessary knowledge and design principles for network equipment like routers, bridges etc.

INSTRUCTIONAL OBJECTIVES
1. To familiarize embedded communication devices.
2. To understand the functions of each communication layer of ISO standard.
3. To learn network processors.

UNIT I - OVERVIEW OF DATA NETWORKS (6 hours)
End point: Data Modems, Serial interfaces, ISDN interface – Communication: Types of switching, Types of error: single and burst error, Error detection, redundancy check: Longitudinal, vertical, and cyclic error correction, architecture of computer network - Overview of OSI reference model – Network components: Routers, Bridges and Gateways.

UNIT II - COMMUNICATION SOFTWARE DESIGN (12 hours)
Ecosystem - embedded communications software - software partitioning - module and task decomposition - Partitioning case study - Protocol software - debugging protocols - tables and other data structures - table access routines - Buffer and timer management - Management software – device & router management – CLI based management & HTTP based management - Agent to protocol interface – device to manager communication – system setup, boot & post-boot configuration – saving and restoring the configuration.

UNIT III - MULTI-BOARD DESIGN (9 hours)
Multiboard common architectures for communication equipment – Single board, chassis and rack-based designs - Components of a multi board designs – RTOS support for distribution – data structure and state machine changes for distribution – failures and fault tolerance in multi board systems.

UNIT IV - DESIGN PRINCIPLES OF SCHEDULING (9 hours)

UNIT V - COMMUNICATION PROCESSOR ARCHITECTURES (9 hours)

REFERENCES
EMBEDDED WIRELESS SENSOR NETWORKS

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Total Contact Hours – 45
Prerequisite : Nil

PURPOSE
Wireless sensor networks are an becoming an important application of embedded systems, giving scope for unique designs and applications. This course is aimed at imparting knowledge on wireless sensor networks and practical implementation.

INSTRUCTIONAL OBJECTIVES
1. To understand the concepts of sensor networks.
2. To learn implementation issues and techniques wireless sensor nodes.

UNIT I - INTRODUCTION TO WSN
Introduction to WSN-Challenges for WSNs - Characteristic requirements - Required mechanisms - Single-node architecture -Hardware components-Energy consumption of sensor nodes-Operating systems and execution environments-Some examples of sensor nodes.

UNIT II - NETWORK ARCHITECTURE
Sensor network scenarios- Optimization goals and figures of merit- Design principles for WSNs, Service interfaces of WSNs- Gateway concepts.

UNIT III - SENSOR NETWORK IMPLEMENTATION

UNIT IV - PROGRAMMING MODELS
An Introduction to the Concept of Cooperating Objects and Sensor Networks- System Architectures and Programming Models.

UNIT V - CASE STUDIES
Wireless sensor networks for environmental monitoring, Wireless sensor networks with mobile nodes, Autonomous robotic teams for surveillance and monitoring, Inter-vehicle communication networks.

REFERENCES
UNIT I - INTRODUCTION (9 hours)
Wireless Transmission-signal propagation-spread spectrum-Satellite Networks-Capacity Allocation-FAMA-DAMA-MAC.

UNIT II - MOBILE NETWORKS (9 hours)

UNIT III - WIRELESS NETWORKS (9 hours)

UNIT IV - ROUTING (9 hours)

UNIT V - TRANSPORT AND APPLICATION LAYERS (9 hours)

REFERENCES
EM2107

EMBEDDED CONTROL SYSTEMS

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Total Contact Hours – 45

Prerequisite: Nil

PURPOSE
To introduce the basic concepts of control systems and its embedded implementation.

INSTRUCTIONAL OBJECTIVES
1. To learn the basics of control systems.
2. To learn control theory as used in embedded systems.
3. To learn application of control systems.
4. To learn I/O devices used in control systems.

UNIT I - CONTROL SYSTEM BASICS (12 hours)
Z-transforms – performance requirements - block diagrams - analysis and design - sampling theory – difference equations.

UNIT II - CONTROL SYSTEM IMPLEMENTATION (9 hours)

UNIT III - CONTROL SYSTEM TESTING (6 hours)
Software implications - Controller implementation and testing in embedded systems - Measuring frequency response.

UNIT IV - INPUT DEVICES (6 hours)
Keyboard basics - Keyboard scanning algorithm - Character LCD modules - LCD module display Configuration - Time-of-day clock - Timer manager - Interrupts - Interrupt service routines - Interrupt-driven pulse width modulation. Triangle waves analog vs. digital values - Auto port detect - Capturing analog information in the timer interrupt service routine - Automatic, multiple channel analog to digital data acquisition.

UNIT V - OUTPUT DEVICES (3 hours)
H Bridge – relay drives - DC/ Stepper Motor control – optical devices.

UNIT VI - SENSORS (7 hours)

UNIT VII - CASE STUDY (2 hours)
Examples for sensor, actuator, control circuits with applications.
REFERENCES

EM2108

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PURPOSE
Intelligent system concepts are becoming more relevant in the embedded systems. To give an overview of design principles and applications this course is offered.

INSTRUCTIONAL OBJECTIVES
1. To learn basic intelligent system concepts.
2. To learn neural networks.
3. To learn fuzzy logic and its implementation methods.

UNIT I - INTRODUCTION AND BASIC CONCEPTS (9 hours)
Introduction- Humans and Computers, the structure of the brain, learning in machines, the differences. The basic neuron- Introduction, modeling the single neuron, learning in simple neurons, the perception: a vectorial perspective, the perception learning rule, proof, limitations of perceptrons.

UNIT II - MULTILAYER NETWORKS (9 hours)
The multi layer perceptron: Introduction, altering the perception model, the new model, the new learning rule, multi layer perception algorithm, XOR problem. Multi layer feed forward networks, error back propagation training algorithm: problems with back propagation, Boltzman training, Cauchy training, combined back propagation, Cauchy training.

UNIT III - RESONANT NETWORKS AND APPLICATIONS (9 hours)

UNIT IV - FUZZY SET THEORY (9 hours)

UNIT V - FUZZY LOGIC AND SYSTEMS (9 hours)
REFERENCES

EM2109

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PURPOSE
Since image processing is an upcoming embedded field wherein many small systems and robots are built with image processing functions we give in this subject an idea of image processing concepts.

INSTRUCTIONAL OBJECTIVES
1. To learn basic Image processing operations and concepts.
2. To learn multi resolution analysis.
3. To study video processing.

UNIT I - FUNDAMENTALS OF IMAGE PROCESSING (9 hours)
Introduction - Steps in image processing systems - Image acquisition - Sampling and Quantization - Pixel relationships - Color fundamentals and models, File formats, Image operations – Arithmetic and Morphological.

UNIT II - IMAGE ENHANCEMENT (9 hours)

UNIT III - IMAGE SEGMENTATION AND FEATURE ANALYSIS (9 hours)
Detection of Discontinuities - Edge operators - Edge linking and Boundary Detection - Thresholding - Region based segmentation - Morphological Watersheds - Motion Segmentation.

UNIT IV - OBJECT RECOGNITION (10 hours)
Introduction – Pattern and Pattern Class – Selection Measurement Parameters – Approaches – Types of Classification – Bayes, Template matching, Non parametric density estimation, Neural Network approach – Applications.
UNIT V - VIDEO PROCESSING  
(8 hours)
Real time image and Video processing – parallelism – Algorithm simplification strategy – Hardware platforms – DSP, FPGA, GPU, General purpose processors.

REFERENCES
EM2110

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Prerequisite :Nil

**PURPOSE**
Multimedia applications are coming in to the arena of embedded systems. With future applications in mind this course on multimedia systems is offered.

**INSTRUCTIONAL OBJECTIVES**
1. To learn multimedia principles.
2. To learn knowledge and user understanding.
3. To study text, sound and image applications.

**UNIT I - MULTIMEDIA** (9 hours)

**UNIT II - KNOWLEDGE AND USER UNDERSTANDING** (9 hours)
Knowledge – Basic idea of knowledge – A working definition – Knowledge representation – Knowledge Elicitation – Know about user applying user knowledge – acquiring user knowledge – User profiling – User modeling.

**UNIT III - INTERACTION, INTERFACE & SEMIOTICS** (9 hours)

**UNIT IV - TEXT AND SOUND** (9 hours)

**UNIT V - IMAGES** (9 hours)

**REFERENCES**
EM2111

DSP INTEGRATED CIRCUITS

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Total Contact Hours – 45

Prerequisite

EM2008 / EM2009

PURPOSE
To impart knowledge of VLSI implementation of DSP circuits.

INSTRUCTIONAL OBJECTIVES

1. To learn implementation of DSP in VLSI.

UNIT I - DSP IC’S AND VLSI CIRCUIT TECHNOLOGIES (9 hours)
Standard digital signal processors, Application specific IC’s for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

UNIT II - DIGITAL SIGNAL PROCESSING (9 hours)

UNIT III - DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS (9 hours)
FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT IV - DSP ARCHITECTURES AND THEIR SYNTHESIS (9 hours)
DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

UNIT V - ARITHMETIC UNITS AND IC DESIGN (9 hours)
Conventional number system, redundant Number system, Residue Number System. Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies.

REFERENCES
PURPOSE
The concepts of real time systems and their analysis is very essential for embedded systems this course if offered.

INSTRUCTIONAL OBJECTIVES
1. To learn real time aspects of OS, memory communication of systems.
2. To study reliability evaluation methods.

UNIT I - INTRODUCTION TO TASK SCHEDULING (9 hours)

UNIT II - UNI AND MULTI PROCESSOR SCHEDULING (9 hours)

UNIT III - REAL TIME COMMUNICATION (9 hours)

UNIT IV - REAL TIME DATABASES (9 hours)
Basic Definition, Real time Vs General purpose databases, Main Memory Databases, Transaction priorities, Transaction Aborts, Concurrency control issues, Disk Scheduling Algorithms, Two-phase Approach to improve Predictability, Maintaining Serialization Consistency, Databases for Hard Real Time System.

UNIT V - REAL-TIME MODELING AND CASE STUDIES (9 hours)
Petrinets and applications in real-time modeling, Air traffic controller system – Distributed air defense system.

REFERENCES
UNIT I - EMISSION AND INTERFERENCE (7 hours)
Conducted, radiated emission – cross talk – shielding theory.

UNIT II - EMC TESTING (6 hours)
RF emissions – immunity tests – low frequency techniques – EMC compliance.

UNIT III - EMC IN DESIGN (6 hours)

UNIT IV - RELIABILITY MATHEMATICS (8 hours)

UNIT V - ELECTRONIC SYSTEM RELIABILITY (6 hours)

UNIT VI - SYSTEM DESIGN (6 hours)
System design – design phases – design styles – design of safety critical systems – design diversity – design for maintainability.

UNIT VII - PRODUCT DESIGN (6 hours)

REFERENCES

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PURPOSE
To present and illustrate an extensive collection of image processing tools to help the user and prospective user of computer-based systems understand the methods provided in various software packages.

INSTRUCTIONAL OBJECTIVES
1. To understand the image fundamentals and mathematical transforms necessary for image Processing and to study the image enhancement techniques.
2. To understand the image segmentation and representation techniques.
3. To understand how image are analyzed to extract features of interest.
4. To introduce the concepts of image registration and image fusion.
5. To analyze the constraints in image processing when dealing with 3D data sets.

UNIT-I: FUNDAMENTALS OF DIGITAL IMAGE PROCESSING (9 hours)
Elements of visual perception, brightness, contrast, hue, saturation, mach band effect, 2D image transforms-DFT, DCT, KLT, and SVD. Image enhancement in spatial and frequency domain, Review of morphological image processing.

UNIT-II: SEGMENTATION (9 hours)
Edge detection, Thresholding, Region growing, Fuzzy clustering, Watershed algorithm, Active contour methods, Texture feature based segmentation; Model based segmentation, Atlas based Segmentation, Wavelet based Segmentation methods.

UNIT-III: FEATURE EXTRACTION (9 hours)
First and second order edge detection operators, Phase congruency, Localized feature extraction detecting image curvature, shape features Hough transform, shape skeletonization, Boundary descriptors, Moments, Texture descriptors- Autocorrelation, Co-occurrence features, Runlength features, Fractal model based features, Gabor filter, wavelet features.

UNIT-IV: REGISTRATION (9 hours)
Registration- Preprocessing, Feature selection-points, lines, regions and templates Feature Correspondence-Point pattern matching, Line matching, and region matching Template matching. Transformation functions-Similarity transformation and Affine Transformation. Resampling- NearestNeighbour and Cubic Splines.
UNIT-V: IMAGE PROCESSING ON 3D (9 hours)
Image fusion – pixel, Multiresolution and region based fusion. 3D image visualization - 3D Data sets, Volumetric display, Stereo Viewing, Ray tracing, Image processing in 3D, Measurements on 3D images.

REFERENCES

EM2115
DIGITAL VIDEO SIGNAL PROCESSING

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Total Contact Hours – 45
Prerequisite: Nil

PURPOSE
Advance in digital multimedia enables to deliver high quality video. As multimedia becomes more pervasive, the boundaries between video, graphics, computer vision, multimedia database starts to blur, making video processing an exciting field. This course intends to address the concept of video representation, video signal and coding.

INSTRUCTIONAL OBJECTIVES
1. To impart knowledge on the basic video signal representation
2. To learn the basic Fourier and frequency analysis of video signals.
3. Video sampling and motion estimation.
4. Coding of video signals and standards.

UNIT-I: VIDEO FORMATION, PERCEPTION AND REPRESENTATION (9 hours)

UNIT-II: FOURIER ANALYSIS OF VIDEO SIGNALS AND FREQUENCY RESPONSE OF THE HUMAN VISUAL SYSTEM (9 hours)
Multidimensional Continuous-Space Signals and Systems, Multidimensional discrete-Space Signals and Systems, Frequency Domain Characterization of Video Signals- Spatial and Temporal Frequencies, Temporal Frequencies Caused by Linear Motion, Frequency Response of

UNIT-III: VIDEO SAMPLING (9 hours)

UNIT-IV: TWO DIMENSIONAL MOTION ESTIMATION (9 hours)
Optical Flow - Two-Dimensional Motion versus Optical Flow, Optical Flow Equation and Ambiguity in Motion Estimation, General Methodologies- Motion Representation, Motion Estimation Criteria, Optimization Methods, Pixel-Based Motion Estimation, Block-Matching Algorithm, Multiresolution Motion estimation.

UNIT-V: WAVEFORM BASED VIDEO CODING AND STANDARDS (9 hours)

REFERENCES

MA2009

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Prerequisite: Nil

PURPOSE
To develop analytical capability and to impart knowledge in Mathematical and Statistical methods and their applications in Engineering and Technology and to apply these concepts in engineering problems they would come across.

INSTRUCTIONAL OBJECTIVES
1. At the end of the course, Students should be able to understand Mathematical and Statistical concepts, Discrete Fourier transform, Z transform, queueing theory concepts and apply the concepts in solving the engineering problems.

UNIT I – BOUNDARY VALUE PROBLEMS (9 hours)
Solution of initial and boundary value problems - Characteristics - D'Alembert's Solution - Significance of Characteristic curves - Laplace transform solutions for displacement in a long string - a long string under its weight - a bar with prescribed force on one end - free vibration of a string.
UNIT II - SPECIAL FUNCTIONS (9 hours)
Series solutions - Bessel's equation - Bessel Functions - Legendre's equation - Legendre Polynomials - Rodrigue's formula - Recurrence relations - Generating Functions and orthogonal property for Bessel functions of the first kind.

UNIT III – DISCRETE TRANSFORMS (9 hours)

UNIT IV - RANDOM VARIABLES (9 hours)
Review of Probability distributions - Random variables - Moment generating functions and their properties - Functions of Random variables.

UNIT V – QUEUEING THEORY (9 hours)
Single and Multiple server Markovian Queueing models - Customer impatience - Queueing applications.

REFERENCES
1. Veerarajan T, "Mathematics IV", Tata McGraw Hill, 2000. (Unit II Chapter 3 Section 3.4 Unit I Chapter 5)
3. Sankara Rao K., "Introduction to Partial Differential Equations", PHI, 1995 (Unit II - Chapter 1, Section 1.3, Chapter 6 Section 6.13)
4. Veerajan T, "Probability, Statistics and Random Processes", 2004 (Unit IV - Chapter 1,2,3,4 Unit V - Chapter 5)
Statistical distribution, statistical confidence and hypothesis testing, probability plotting techniques - Weibull, extreme value, hazard, binomial data; Analysis of load - strength interference, Safety margin and loading roughness on reliability.

UNIT II - STATISTICAL EXPERIMENTS (9 hours)
Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis, Petri Nets, State space Analysis, Monte Carlo simulation, Design analysis methods - quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III - ELECTRONIC SYSTEMS AND SOFTWARE RELIABILITY (9 hours)
Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV - RELIABILITY TESTING (9 hours)
Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V - RELIABILITY IN MANUFACTURE AND MAINTENANCE (9 hours)
Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programmes, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

REFERENCES

VL2113

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Total Contact Hours - 45
Prerequisite : Nil

PURPOSE
MEMS technology offers many exciting opportunities in miniaturization of elements in a wide range of applications. MEMS based sensors and actuators are constantly introduced into new products and new markets are expected to become affected by MEMS technology in the near future. The diversity and complexity of this technology demands a wide knowledge base from a prospect researcher. The goal of this course is to provide the student the needed background to comprehend existing technology, the tools to execute MEMS fabrication and the expertise to approach the development of new MEMS tools.

INSTRUCTIONAL OBJECTIVES
1. To familiarize with MEMS Materials and Scaling Laws in Miniaturization.
3. To study Microsystems Fabrication Process.
4. To familiarize with Microsystems Design, Assembly and Packaging.
5. To explore on various Case Study of MEMS Devices.

UNIT I - OVERVIEW OF MEMS AND MICROSYSTEMS, MEMS MATERIALS AND SCALING LAWS IN MINIATURATION (9 hours)

UNIT II - ENGINEERING MECHANICS AND THERMOFLUID ENGINEERING FOR MICROSYSTEMS DESIGN (9 hours)

UNIT III - MICROSYSTEMS FABRICATION PROCESS (9 hours)

UNIT IV - MICROSYSTEMS DESIGN, ASSEMBLY AND PACKAGING (9 hours)
Micro system Design - Design consideration, process design, Mechanical design, Mechanical design using MEMS. Mechanical packaging of Microsystems, Microsystems packaging, interfacings in Microsystems packaging, packaging technology, selection of packaging materials, signal mapping and transduction.

UNIT V - CASE STUDY OF MEMS DEVICES (9 hours)
Case study on strain sensors, Temperature sensors, Pressure sensors, Humidity sensors, Accelerometers, Gyroscopes, RF MEMS Switch, phase shifter, and smart sensors. Case study of MEMS pressure sensor Packaging.

REFERENCES
**PURPOSE**
To enhance holistic development of students and improve their employability skills

**INSTRUCTIONAL OBJECTIVES**
1. To improve aptitude, problem solving skills and reasoning ability of the student.
2. To collectively solve problems in teams & group.
3. Understand the importance of verbal and written communication in the workplace
4. Understand the significance of oral presentations, and when they may be used
5. Practice verbal communication by making a technical presentation to the class
6. Develop time management Skills

**UNIT I–BASIC NUMERACY:** Types and Properties of Numbers, LCM, GCD, Fractions and decimals, Surds

**UNIT II-ARITHMETIC – I:** Percentages, Profit & Loss, Equations

**UNIT III-REASONING – I:** Logical Reasoning

**UNIT IV-SOFT SKILLS – I:** Presentation skills, E-mail Etiquette

**UNIT V-SOFT SKILLS – II:** Goal Setting and Prioritizing

**ASSESSMENT**

**Soft Skills (Internal)**
Assessment of presentation and writing skills.

**Quantitative Aptitude (External)**
- Objective Questions- 60 marks
- Descriptive case lets- 40 marks*
- Duration: 3 hours

*Engineering problems will be given as descriptive case lets.

**REFERENCES**
1. Quantitative Aptitude by Dinesh Khattar – Pearson’s Publicaitons
2. Quantitative Aptitude and Reasoning by RV Praveen – EEE Publications
4. Soft Skills for Everyone by Jeff Butterfield – Cengage Learning India Private Limited
5. Six Thinking Hats is a book by Edward de Bono - Little Brown and Company
6. IBPS PO - CWE Success Master by Arihant - Arihant Publications(I) Pvt.Ltd - Meerut
PURPOSE
To enhance holistic development of students and improve their employability skills

INSTRUCTIONAL OBJECTIVES
1. To improve aptitude, problem solving skills and reasoning ability of the student
2. To collectively solve problems in teams & group
3. Understand the importance of verbal communication in the workplace
4. Understand the significance of oral presentations, and when they may be used
5. Understand the fundamentals of listening and how one can present in a group discussion
6. Prepare or update resume according to the tips presented in class

UNIT I - ARITHMETIC – II: Ratios & Proportions, Mixtures & Solutions

UNIT II - MODERN MATHEMATICS: Sets & Functions, Data Interpretation, Data Sufficiency

UNIT III – REASONING – II: Analytical Reasoning

UNIT IV – COMMUNICATION – I: Group discussion, Personal interview

UNIT V - COMMUNICATION – II: Verbal Reasoning test papers

ASSESSMENT

1. Communication (Internal)
   - Individuals are put through formal GD and personal interviews.
   - Comprehensive assessment of individuals’ performance in GD & PI will be carried out.

2. Quantitative Aptitude (External)
   - Objective Questions- 60 marks (30 Verbal +30 Quants)
   - Descriptive case lets- 40 marks*
   - Duration: 3 hours
   *Engineering problems will be given as descriptive case lets.

REFERENCES
1. Quantitative Aptitude by Dinesh Khattar – Pearsons Publicaitons
2. Quantitative Aptitude and Reasoning by RV Praveen – EEE Publications
3. Quantitative Aptitude by Abijith Guha – TATA Mc GRAW Hill Publications
4. General English for Competitive Examination by A.P. Bharadwaj – Pearson Educaiton
5. English for Competitive Examination by Showick Thorpe - Pearson Educaiton
6. IBPS PO - CWE Success Master by Arihant - Arihant Publications(I) Pvt.Ltd - Meerut
7. Verbal Ability for CAT by Sujith Kumar - Pearson India
8. Verbal Ability & Reading Comprehension by Arun Sharma - Tata McGraw - Hill Education
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**PURPOSE**
To develop professional skills abreast with contemporary teaching learning methodologies

**INSTRUCTIONAL OBJECTIVES**
At the end of the course the student will be able to

1. acquire knowledge on planning, preparing and designing a learning program
2. prepare effective learning resources for active practice sessions
3. facilitate active learning with new methodologies and approaches
4. create balanced assessment tools
5. hone teaching skills for further enrichment

**UNIT-I: DESIGN**
Planning & Preparing a learning program, Planning & Preparing a learning session (2 hrs)

**UNIT-II: PRACTICE**
Facilitating active learning, Engaging learners (2 hrs)

**UNIT-III: ASSESSMENT**
Assessing learner’s progress, Assessing learner’s achievement (2 hrs)

**UNIT-IV: HANDS ON TRAINING**
Group activities – designing learning session, Designing teaching learning resources, Designing assessment tools, Mock teaching session (10 hrs)

**UNIT-V: TEACHING IN ACTION**
Live teaching sessions, Assessments (14 hrs)

**ASSESSMENT (Internal)**

Weightage:

- Design - 40%
- Practice – 40%
- Quiz – 10%
- Assessment – 10%

**REFERENCES**
1. Cambridge International Diploma for Teachers and Trainers Text book by Ian Barker - Foundation books

#
Every student will be required to present a seminar talk on a topic approved by the Department. The Committee constituted by the Head of the Department will evaluate the presentation and will award the marks based on

- Comprehensible arguments and organization.
- Accessible delivery
- Accessible visuals in support of arguments.
- Question and Answers.

Student has to identify the faculty supervisor (Guide), topic, objectives, deliverables and work plan. The topic should be of advanced standing requiring use of knowledge from program core and be preferably hardware oriented. Students are evaluated on monthly basis, by conducting reviews by the department throughout the project period. Student has to submit a report describing his/her project work. End semester examination/ Viva-voce will be conducted by the Department.

Student has to continue the project work he/she was doing in phase –I. The Student will be evaluated with monthly reviews and an end semester examination / viva-voce. The students are encouraged to submit his/her project work in Conference/Journal and due weightage will be given in their evaluation.
### AMENDMENTS

<table>
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<tr>
<th>S.No.</th>
<th>Details of Amendment</th>
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<th>Approval with date</th>
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<tr>
<td>1.</td>
<td>EM2114</td>
<td>29-Aug-2015</td>
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<td></td>
<td>29th Academic Council Meeting (ACM), Agenda No. 3.3.19</td>
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<td>2.</td>
<td>EM2115</td>
<td>24-Mar-2016</td>
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<td>31st ACM, Agenda No. 3.3.10</td>
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